What is claimed is:

1. A method for depositing tungsten nitride, comprising the following steps:

a) providing a source gas mixture capable of depositing the tungsten nitride;

b) combining a silicon containing gas with the source gas mixture to form a source gas mixture comprising the silicon containing gas;

c) applying a temperature to a deposition substrate;

d) applying a pressure to the source gas mixture comprising the silicon containing gas; and

e) depositing the tungsten nitride from the source gas mixture comprising the silicon containing gas to overlie said deposition substrate.

2. The method as specified in Claim 1, further comprising the step of maintaining a temperature of interior walls of a deposition chamber containing said source gas mixture comprising the silicon containing gas at a temperature greater than 25 degrees Celsius.

3. The method as specified in Claim 1, further comprising the step of maintaining a temperature of interior walls of a deposition chamber containing said source gas mixture comprising the silicon containing gas at a temperature which minimizes adduct formation during said step of depositing.

4. The method as specified in Claim 1, further comprising the step of filling a via during said step of depositing to form an electrical contact in the via.

5. The method as specified in Claim 1, further comprising the following steps:

a) lining sides of a via during said step of depositing to form a barrier layer of tungsten nitride; and

b) filling remaining portions of the via with tungsten, the tungsten nitride and the tungsten forming an electrical contact.

6. The method as specified in Claim 1, further comprising the following steps:

a) creating a first capacitor electrode;

b) creating a dielectric layer overlying said first capacitor electrode; and

c) forming a second capacitor electrode during said step of depositing the tungsten nitride such that said tungsten nitride overlies the dielectric layer thereby forming the second capacitor electrode.

7. The method as specified in Claim 1, further comprising the following steps:

a) creating a first capacitor electrode;

b) creating a dielectric layer of tantalum oxide overlying said first capacitor electrode; and

c) forming a second capacitor electrode during said step of depositing the tungsten nitride such that said tungsten nitride overlies the layer of tantalum oxide thereby forming the second capacitor electrode.

8. The method as specified in Claim 1, further comprising the following steps:

a) forming a first capacitor electrode during said step of depositing the tungsten nitride;

b) creating a dielectric layer of tantalum oxide overlying said first capacitor electrode; and

c) creating a second capacitor electrode overlying said dielectric layer.

9. The method as specified in Claim 1, wherein said step of providing comprises the step of combining at least tungsten hexaflouride, ammonia, argon, and hydrogen to form the source gas mixture.

10. The method as specified in Claim 1, further comprising the step of interposing the tungsten nitride between a polysilicon layer and a tungsten layer, said polysilicon layer, said tungsten nitride, and said tungsten layer forming a gate electrode.

11. The method as specified in Claim 1, further comprising adjusting a flow rate of the silicon containing gas to be within the range of .1% to 25 % of a total flow rate of the source gas mixture comprising the silicon containing gas.

12. A method for depositing tungsten nitride, comprising the following steps:

a) providing a source gas mixture capable of depositing tungsten nitride;

b) combining silane with the source gas mixture to form a source gas mixture comprising the silane;

c) applying a temperature to a deposition substrate;

d) applying a pressure to the source gas mixture comprising the silane; and

e) depositing the tungsten nitride from the source gas mixture comprising the silane onto said deposition substrate.

13. The method as specified in Claim 12, further comprising the step of adjusting a flow rate of the silane to be within the range of .1 to 25 % of a total flow rate of the source gas mixture comprising the silane.

14. The method as specified in Claim 12, further comprising the step of selecting the silane from a group consisting of organic silane and a silane which is a multiple order of silane.

15. A semiconductor non-planar storage capacitor, comprising:

a) a non-planar first capacitor electrode;

b) a dielectric layer overlying said first capacitor electrode; and

c) a tungsten nitride layer overlying said dielectric layer, said tungsten nitride layer forming a second capacitor electrode of the non-planar storage capacitor.

16. The non-planar storage capacitor as specified in Claim 15, wherein said dielectric layer is tantalum oxide.

17. The non-planar storage capacitor as specified in Claim 15, wherein said tungsten nitride layer comprises silicon.

18. The non-planar storage capacitor as specified in Claim 15, wherein said first capacitor electrode is tungsten nitride.

19. A semiconductor non-planar storage capacitor, comprising:

a) a non-planar first capacitor electrode of tungsten nitride;

b) a dielectric layer overlying said first capacitor electrode; and

c) a second capacitor electrode overlying said dielectric layer.

20. A method for forming a semiconductor non-planar storage capacitor, comprising the following steps:

a) creating a non-planar first capacitor electrode overlying a deposition substrate;

b) creating a dielectric layer overlying said first capacitor electrode;

c) creating a source gas mixture for depositing tungsten nitride; and

d) depositing the tungsten nitride from the source gas mixture to form a second capacitor electrode of tungsten nitride overlying said dielectric layer.

21. The method as specified in Claim 20, wherein said step of creating said dielectric layer comprises depositing a layer of tantalum oxide.

22. The method as specified in Claim 20, wherein said step of creating the source gas mixture comprises combining at least tungsten hexaflouride, ammonia, argon, and hydrogen to form the source gas mixture.

23. The method as specified in Claim 20, wherein said step of creating the source gas mixture comprises combining at least tungsten hexaflouride, ammonia, argon, hydrogen, and a silicon containing gas to form the source gas mixture.

24. The method as specified in Claim 23, further comprising adjusting a flow rate of the silicon containing gas to be within the range of .1% to 25 % of a total flow rate of the source gas mixture.

25. The method as specified in Claim 20, wherein said step of creating the source gas mixture comprises combining at least tungsten hexaflouride, ammonia, argon, hydrogen, and a silane to form the source gas mixture.

26. The method as specified in Claim 25, further comprising adjusting a flow rate of the silane to be within the range of .1% to 25 % of a total flow rate of the source gas mixture.

27. The method as specified in Claim 20, further comprising the following steps:

a) creating the source gas mixture in a chamber; and

b) adjusting a temperature of interior walls of the chamber to a temperature greater than 25 degrees Celsius.

28. The method as specified in Claim 20, further comprising the following steps:

a) creating the source gas mixture in a chamber; and

b) adjusting a temperature of interior walls of the chamber to a temperature which minimizes adduct formation during said step of depositing.

29. A non-planar capacitor fabricated according to a process comprising the following steps:

a) creating a non-planar first capacitor electrode overlying a deposition substrate;

b) creating a dielectric layer overlying said first capacitor electrode;

c) providing a source gas mixture capable of depositing tungsten nitride;

d) combining a silicon containing gas with the source gas mixture to form a source gas mixture comprising the silicon containing gas;

e) applying a temperature to the deposition substrate;

f) applying a pressure to the source gas mixture comprising the silicon containing gas; and

g) depositing the tungsten nitride from the source gas mixture comprising the silicon containing gas to form a second capacitor electrode of tungsten nitride overlying the dielectric layer.

30. The non-planar capacitor as specified in Claim 29, wherein said dielectric layer is tantalum oxide.

31. The non-planar capacitor as specified in Claim 29, wherein said silicon containing gas is silane.

32. The non-planar capacitor as specified in Claim 29, wherein said tungsten nitride comprises silicon.

33. The non-planar capacitor as specified in Claim 29, further comprising adjusting a flow rate of the silicon contaming gas to be within the range of .1% to 25% of a total flow rate of the source gas mixture comprising the silicon containing gas.

34. A capacitor electrode made by the process comprising the following steps:

a) providing a source gas mixture capable of depositing tungsten nitride;

b) combining a silicon containing gas with the source gas mixture to form a source gas mixture comprising the silicon containing gas;

c) applymg a temperature to a deposition substrate;

d) applying a pressure to the source gas mixture comprising the silicon containing gas; and

e) depositing tungsten nitride from the source gas mixture comprising the silicon containing gas to form the capacitor electrode overlying the deposition substrate.

35. A gate electrode made by the process comprising the following steps:

a) providing a source gas mixture capable of depositing tungsten nitride;

b) combining a silicon containing gas with the source gas mixture to form a source gas mixture comprising the silicon containing gas;

c) applying a temperature to a deposition substrate;

d) applying a pressure to the source gas mixture comprising the silicon containing gas;

e) depositing the tungsten nitride from the source gas mixture comprising the silicon containing gas to form a tungsten nitride layer overlying the deposition substrate;

f) creating a tungsten layer overlying the tungsten nitride layer;

g) patterning the tungsten nitride layer and the tungsten layer to define

the gate electrode; and

h) removing unmasked portions of the tungsten nitride layer and the tungsten layer, portions of the tungsten nitride layer and the tungsten layer remaining after the step of removing forming the gate electrode.

36. A gate electrode made by the process comprising the following steps:

a) creating a polycrystalline silicon layer overlying a deposition substrate;

b) providing a source gas mixture capable of depositing a tungsten nitride;

c) combining a silicon containing gas with the source gas mixture to form a source gas mixture comprising the silicon containing gas;

d) applying a temperature to the deposition substrate;

e) applying a pressure to the source gas mixture comprising the silicon containing gas;

f) depositing the tungsten nitride from the source gas mixture comprising the silicon containing gas to form a tungsten nitride layer overlying the polycrystalline silicon layer;

g) creating a tungsten layer overlying the tungsten nitride layer;

h) patterning the polycrystalline silicon layer, the tungsten nitride layer, and the tungsten layer to define the gate electrode; and

i) removing unmasked portions of the polycrystalline silicon layer, the tungsten nitride layer and the tungsten layer, portions of the polycrystalline silicon layer, the tungsten nitride layer, and the tungsten layer remaining after the step of removing forming the gate electrode.

37. A deposition in a via made by the process comprising the following steps:

a) providing a source gas mixture capable of depositing tungsten nitride;

b) combining a silicon containing gas with the source gas mixture to form a source gas mixture comprising the silicon containing gas;

c) applying a temperature to a deposition substrate;

d) applying a pressure to the source gas mixture comprising the silicon containing gas; and

e) depositing the tungsten nitride from the source gas mixture comprising the silicon containing gas to form the deposition in the via.

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38. An integrated circuit capacitor comprising:

a first electrode formed of polysilicon;

a second electrode formed of chemically vapor deposited tungsten nitride formed using a gas comprising nitride, tungsten and silicon; and

a dielectric layer located between the first and second electrodes.

39. The integrated circuit capacitor of claim 38 wherein the dielectric layer is comprised of tantalum oxide.

40. The integrated circuit capacitor of claim 38 wherein the capacitor is a memory cell.

41. A capacitor, comprising:

a first electrode;

a second electrode; and

a dielectric disposed between the first and the second electrode,

wherein at least one of the first electrode and the second electrode includes only tungsten nitride.

42. The capacitor of claim 41, wherein both the first electrode and the second electrode includes only tungsten nitride.

43. The capacitor of claim 41, wherein the capacitor is a non-planar capacitor.

44. The capacitor of claim 41, wherein the dielectric includes tantalum oxide.

45. The capacitor of claim 41, wherein the tungsten nitride prevents degradation of the dielectric.

46. A capacitor, comprising:

a first electrode;

a dielectric disposed on the first electrode; and

a second electrode formed on the dielectric as a layer of only tungsten nitride.

47. The capacitor of claim 46, wherein the capacitor is a non-planar capacitor.

48. The capacitor of claim 46, wherein the dielectric includes tantalum oxide.

49. The capacitor of claim 46, wherein the layer of only tungsten nitride is conformally deposited by chemical vapor deposition.

50. The capacitor of claim 46, wherein the layer of only tungsten nitride is exposed to silicon based materials, and wherein a boundary between the layer of only tungsten nitride and the silicon based materials is characterized by a reduced encroachment of the tungsten nitride into the silicon based materials.

51. The capacitor of claim 46, wherein the first electrode is formed as a conformal polycrystalline silicon layer.

52. A capacitor, comprising:

a first electrode formed as a layer of only tungsten nitride;

a dielectric disposed on the first electrode; and

a second electrode formed on the dielectric.

53. The capacitor of claim 52, wherein the capacitor is a non-planar capacitor.

54. The capacitor of claim 52, wherein the dielectric includes tantalum oxide.

55. The capacitor of claim 52, wherein the layer of only tungsten nitride is conformally deposited by chemical vapor deposition.

56. The capacitor of claim 52, wherein the layer of only tungsten nitride is exposed to silicon based materials, and wherein a boundary between the layer of only tungsten nitride and the silicon based materials is characterized by a reduced encroachment of the tungsten nitride into the silicon based materials.

57. The capacitor of claim 52, wherein the second electrode is formed as a polycrystalline silicon layer.

58. A non-planar capacitor, comprising:
a polycrystalline silicon film;
a dielectric layer disposed on the polycrystalline film; and
a film of only tungsten nitride disposed on the dielectric layer.

59. The non-planar capacitor of claim 58, wherein the polycrystalline silicon film is a conformal film formed over a substrate and over transistor devices on the substrate.

60. The non-planar capacitor of claim 58, wherein the dielectric layer includes tantalum oxide.

61. The non-planar capacitor of claim 58, wherein the film of only tungsten nitride is conformally deposited by chemical vapor deposition.

62. A non-planar capacitor, comprising:

a conformal polycrystalline silicon film formed over a substrate and over transistor devices on the substrate;

a dielectric layer formed on the conformal polycrystalline silicon film; and

a film of only tungsten nitride conformally deposited on the dielectric layer by chemical vapor deposition.

63. The non-planar capacitor of claim 62, wherein the film of only tungsten nitride is formed by a chemical vapor deposition process that uses ammonia as a source of nitrogen and a gas selected from the group consisting of tungsten hexaflouride and tungsten carbonyl as a source of tungsten.

64. The non-planar capacitor of claim 62, wherein the film of only tungsten nitride is formed by a chemical vapor deposition process that uses a source gas mixture that includes:

ammonia;

a gas selected from the group consisting of tungsten hexaflouride and tungsten carbonyl; and

a gas selected from the group consisting of silane, organic silane, and a compound that is a multiple order of silane.

65. The non-planar capacitor of claim 62, wherein the dielectric layer includes tantalum oxide.

66. A non-planar capacitor, comprising:

a first electrode;

a dielectric layer formed on the first electrode; and

a film of only tungsten nitride conformally deposited on the dielectric layer by chemical vapor deposition that uses gases, including:

ammonia;

a gas selected from the group consisting of tungsten hexaflouride and tungsten carbonyl; and

a gas selected from the group consisting of silane, organic silane, and a compound that is a multiple order of silane.

67. The non-planar capacitor of claim 66, wherein the first electrode includes a conformal polycrystalline silicon film formed over a substrate and over transistor devices on the substrate.

68. The non-planar capacitor of claim 66, wherein the gases used in the chemical vapor deposition process are a source gas mixture.

69. An integrated circuit, comprising:

a substrate;

at least one transistor device formed on the substrate and arranged to leave a contact area with the substrate;

a non-planar capacitor, including:

a first electrode;

a second electrode; and

a dielectric disposed between the first and the second electrode,

wherein at least one of the first electrode and the second electrode includes only tungsten nitride.

70. The integrated circuit of claim 69, wherein both the first electrode and the second electrode includes only tungsten nitride.

71. The integrated circuit of claim 69, wherein the first electrode includes only tungsten nitride.

72. The integrated circuit of claim 69, wherein the second electrode includes only tungsten nitride.

73. The integrated circuit of claim 69, wherein the dielectric includes tantalum oxide.

74. The integrated circuit of claim 69, wherein the tungsten nitride prevents degradation of the dielectric.